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With separately available socket modules, you purchase only what you, guides users through the extensive tool capabilities without their having to access instruction manuals New devices are supported upon their introduction via software upgrades. Updates are posted on Intel Chapters 3 through 7 describe the processors programming environment, which includes the instruction execution environment, data types, addressing modes, floating point operations and instruction set. Chapters They are developed and manufactured by using a broad range of processes and methods. Programmer which is providing, of mass production,Gang Programmer SU2000 is the revolutionized product released in the mid 1997, enhance our product spreading is welcome.Intel s CHMOS process provides a high, on the 87C196KB. With a 16 MHz oscillator a 16bit addition takes 0.50 jus, and the instruction times, Manufacturer Hill.Intel s CHMOS process provides a high performance processor along with low power consumption.PROGRAMMER S GUIDE AND INSTRUCTION SET Memory Organization Program Memory The 80C51, 1995 243 Philips Semiconductors 80C51 family programmer s guide and instruction set, Semiconductors 80C51 family programmer s guide and instruction set 80C51 Family Table 1. SYMBOL, programmer s guide and instruction set 80C51 Family INTERRUPTS To use any of the interrupts in the PROGRAMMER S GUIDE AND INSTRUCTION SET Memory Organization Program Memory The 80C51, Sep 18 1 Philips Semiconductors 80C51 family programmer s guide and instruction set, Semiconductors 80C51 family programmer s guide and instruction set 80C51 Family Table 1. SYMBOL, Map 1997 Sep 18 4 Philips Semiconductors 80C51 family programmer s guide and instruction Chapters 8 through 16

describe the facilities to support kernel functions, instruction set, organized in alphabetical order.http://kitchensofdiablo.com/upload/camera-sony-w210-manual.xml

Table 11 shows those chapters that will be of most Verify with your local Intel sales office that you have the latest datasheet before finalizing a design, provided in connection with Intel products. Intel products are not intended for use. You may have to register before you can post click the register link above to proceed. To start viewing messages, select the forum that you want to visit from the selection below. To participate you need to register. Registration is free. Click here to register now. For a better experience, please enable JavaScript in your browser before proceeding. It may not display this or other websites correctly. You should upgrade or use an alternative browser. I have a 32KB ROM for an 87C196KD and Im getting strange results IDA seems to sometimes be disassembling data as code, for example. From what Ive read in the users manual, the ROM is mapped in at 0x2000, with the reset vector at 0x2080. Is that correct Should the ROM start address be set to 0x2000 Colin By continuing to use this site, you are consenting to our use of cookies. For a better experience, please enable JavaScript in your browser before proceeding. It may not display this or other websites correctly. You should upgrade or use an alternative browser. Nice to meet you all. One of my learning tasks is so i I decided it disassembling a 256kb flash image, a.bin file. The information I have is The target processor belongs to Intels 87c196 family The target EEPROM for the.bin file is a 29F200 one Ive tried the IDA and binwalk programs on the.bin, but with no success. Therefore I am going with the manual, hard method. And here is where I want to ask you how to proceed. Any clues about how to start. I am not able to tell apart code sections from data sections. I have downloaded some user guides for similar chips, but they do not seem to mention this kind of info where the instructions shall be located on an external memory chip.

Thanks a lot in advance; any little piece of help will be much appreciated. DISCLAIMER this is just a learningpurposes project. I am not trying to publish any of my results nor take monetary profit of closed and copyrighted code in any way. IIRC the power on reset address is at an address like 0x2080. Usually when they do this in an architecture they put RAM at address 0x0000. For multibyte instructions on a CISC machine you have to start with the RESET vector and work your way through. The code begins at 2080H. The next instruction word is likely the beginning of a new function or subroutine. This can be confirmed by finding CALL instructions with that destination address. I have actually learnt something. On the other hand, it seems IDA was failing because I was selecting 80196 instead of 80196NP as the target processor. Now I am obtaining a code listing, pretty large by the way. I have confirmed in official docs that the reset vector is located at 0x2080, just as you said. However, when looking into the disassembled file, I can see these at that position ROM2080 start. ROM2080 rst. ROM2080; End of function startI will keep working. PTS Mode Selection Bits PTSCON Bits 75 Figure 512. A Generic PWM Waveform Figure 516. EPA and PTS Operations for the PWM Toggle Mode Example Figure 518. Receiving a Message for Message Object 15 — CPU Flow Figure 1224. Receiving a Message — CAN Controller Flow Figure 1225. Transmitting a Message — CPU Flow Figure 1226. Transmitting a Message — CAN Controller Flow Figure 131. Minimum Hardware Connections Figure 132. Power and Return Connections Figure 133. Onchip Oscillator Circuit Figure 134. External Crystal Connections Figure 135. External Clock Connections Figure 136. External Clock Drive Waveforms Figure 137. Reset Timing Sequence Figure 138. Internal Reset Circuitry Figure 139. Minimum Reset Circuit Figure 1310. Write Strobe Mode Figure 1514. 16bit System with Singlebyte Writes to RAM Figure 1515.

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Address Valid Strobe Mode Figure 1516. Timings of Address Valid with Write Strobe Mode Figure 1520. 16bit System with RAM Figure 1521. Modes 0, 1, 2, and 3 Timings Figure 1522. Mode 1 System Bus Timing Figure 1523. Mode 2 System Bus Timing Figure 1524. Dump Word Routine Figure 1611. Dump Word Waveform Figure 1612. Auto Programming Circuit for 8XC196K x Devices

Figure 1613. Auto Programming Routine Figure 1614. Serial Port Programming Mode Circuit Figure 1615. Selecting a Window of Upper Register RAM — 8XC196JV Only Table 411. Comparison of PWM Modes Table 513. PWM Toggle Mode PTSCB Table 514. Port Pin States After Reset and After Example Code Execution Table 611. Ports 3 and 4 Pins Table 612. Ports 3 and 4 Control and Status Registers Table 613. Bit Timing Relationships Table 1211. Bit Timing Requirements for Synchronization Table 1212. Control Register Bitpair Interpretation Table 1213. Crossreference for Register Bits Shown in Flowcharts Table 1214. Timing Mnemonics Table 1611. Auto Programming Memory Map Table 1612. Serial Port Programming Mode Memory Map Table 1613. Serial Port Programming Default Values and Locations Table 1614. User Program Register Values and Test ROM Locations Table 1615. EPA Interrupt Priority Vectors Table C15. Specialfunction Signals for Ports 1, 2, 5, 6 Table C18. TIMER x Addresses and Reset Values Table C24. WSR Settings and Direct Addresses for Windowable SFRs U ser ’ s M a nual Includes 8XC196KQ, 8XC196KR, 8XC196KS, 8XC196KT, 8XC196JQ, 8XC196JR, 8XC196JT, 8XC196JV, 87C196CA Intel as sumes no li ability w hatsoever, i n cl udin g infringem ent of an y patent or co p yright, fo r sale and use o f Intel products exc ept as provi ded in Intel’s T erms and Co nditi o ns of S ale for such products. Intel Corporation ma kes no warr anty fo r the use of its products and as sumes no responsib ility fo r any er r ors which may ap pear in this docume nt nor doe s it make a com mitment to update the i nformat ion conta ine d herein.

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This integrated peri pheral is simi lar to Intel’ s s t anda lone 8 2 527 CAN serial communic ations control ler, supp ort ing both t he s tandard and exte nde d me ssage frame s spe cifie d by t he CAN 2.0 protoc ol pa rts A a nd B. Chapter 13 — Minimum Hard ware Consideration s — de scri bes opti o ns for prov iding the ba sic requirem ent s for device operati on within a system, discuss es other hardware considerat i ons, and descri bes devic e reset options. Chapter 1 4 — Sp ecial Ope ratin g Modes — provides an overvie w of the idle, p o wer down, and oncircuit emul ation ONCE modes and describe s how t o enter and exit each mode. Chapter 15 — Interfac ing with Exter nal Me mor y — l i sts the externa l memory signals and de scribes the registers tha t control the external me mory

interface. It discuss es the bus wi dth a nd memory c onfigurations, the bushold protocol, writecontrol modes, and inte rnal wa it sta tes an d ready control. Final ly, i t provides ti min g informatio n for the system bus. Chapter 1 6 — Programming t he Nonvolatile M emory — provide s recomm ended circuits, the corresponding memory maps, and flow diagrams. It also provides procedures f o r auto pr o gram ming, a nd describes t he comm ands used for serial port programming. Appendix A — In struc tion Set Refe rence — pr ovides referenc e inf ormation for the instr uction set.I t also incl ude s t abl es that list the win dowed direct ad d resse s for all SFRs i n e ach possible wi ndow. Glossary — define s term s wi th specia l meaning used th ro ughout thi s ma nual. When use d wi th a signa l name, t he symbol means t hat the signa l is ac tive l o w. W hen used i n an inst ruct ion, t he symbol prefixe s an imm edi ate val ue in i mm edia te a d dressin g mode. Assert a nd De asser t The te rms assert an d de assert refer t o the act of m aki ng a signal active ena bled and inac tive dis able d, respe ctivel y.

Clear an d Se t The terms cl ear and se t refer to the value of a bit or the act of giving it a value. I f a bit is cle ar, its val ue is “0”; c leari ng a bit give s it a “0” value. If a bit is set, i ts value is “1”; settin g a b i t gives i t a “1” value. Instructi o ns Instruct ion mnem onics are shown in uppe r case to av oid confusio n. Y ou may use e ither upper case or lowe r case.The context in which italics are used distinguishe s betwe en the two possi ble meani ngs. V ariable s in regist ers and signal names a re commonl y represented by x and y, where x re prese nts t he first va ria ble a nd y represents the seco n d variable. V ariabl es mus t be repla ced with the c orrect values when c onfig u rin g or programmi ng regist ers or i denti fying si gna ls. De cimal and binary numbe rs are represente d by thei r cus toma ry nota tio n s. That is, 2 55 is a dec imal number a n d 1 11 1 1111 i s a b i nary number. In some c ases, t he lett er B is appended to binary numbers for clarit y. Register B its Bit locatio n s are i ndexe d by 70 o r 150, where bit 0 i s the l east signific ant bit and bit 7 or 15 is the most signi fic ant bit. An individual bit is repres ented by the regis ter name, followe d by a period and t he bit num ber. For e xample, W SR.7 is bi t 7 of the window selec tion regi ster. In some discuss ions, bit name s are use d. Register Nam es Regis ter mnemo nics are show n i n u pper ca se. For exa mple, TIM ER 2 is the tim er 2 regis ter; ti mer 2 i s the ti mer. A regi ster na me cont aining a lowercase italic characte r represents more than one regist er. Reserve d B i ts Certa in bi ts are desc ribe d as reserv ed bit s. In il lust rat ions, rese r ved bits are indicat ed with a dash —. These bit s are not used in this device, but they may be used in future impl ementa tions.

T o help ensure t hat a current s oft ware de sign is compa tible with future i mple menta tions, reser ved bits should be c leare d given a value of “0” or left in t hei r default state s, unless otherwis e noted. Signal Nam es Signal names are shown in upper c ase. When seve ral s ignal s share a commo n nam e, an individ ual si gnal is repre sented by t he signa l name followed by a numbe r. For exampl e, the EP A signals a re name d EP A0, EP A1, EP A2, etc.The value m ay be either binary or hexadecima l, depen d ing on the c onte xt. For exampl e, 2XAFH hex indicates th at bi ts 1 18 are unknown; 10XX in bi nary context indi cates t hat t he t wo L SB s a re u nknown. 1.3 RE L ATED D OCUME NTS The ta ble s in thi s sect ion lis t addit ional docume nts tha t you m ay find use ful in desi gning system s incorporat ing M CS 96 mi crocontrol lers. T hese are not compre hensi ve list s, but are a repres enta tive sample of re levant documents. For a com plete l ist of ava ilable printed docum ents, please or der the lit erature c atalo g order number 21062 1. T o order documents, please c all the Int el lit erature center for y our area telephon e numbers ar e li st ed on page 1 1 1. In te l’ s Ap BUIL DER soft ware, hypertext manua ls and d a tashee ts, and electr onic versions of ap plicatio n note s and c ode e xamples a re als o a vailable f rom t he BBS se e “Bulletin B oard Syst em BBS” on page 19. Ne w in form ation is a vaila ble fi rst from FaxBa ck a nd the BB S. Refer t o “El e c tron i c Supp ort System s” o n page 18 for details. Just dial the telephone numbe r and respond to the system pr o mpts. Afte r you select a d o c ument, the system sen d s a copy to your fax machine. Each doc ument is assigne d an order number an d is listed in a subject c atal og. The first time you use FaxBa ck, you should order the appropr i ate subject catalogs to ge t a complete

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C atalogs are u pda ted twic e monthly, s o call for the latest i nfor m a t ion.The BBS file lis t ing is also available from FaxBack catalog n umber 6; s ee page 18 for phone numbers and a descri ption of the FaxBa ck servic e. 1 80089 72536 U.S. an d C anada on ly An y custome r with a modem and computer can acce ss the BBS. The system provides automatic configuration s upport for 1200 through 19200baud m odems. T ypic al modem s ett ings are 14400 baud, no p a rity, 8 da ta bits, and 1 stop bit 14400, N, 8, 1. T o acce ss the BBS, just dial the tel ephone number and resp ond to th e syste m prompts. During your first session, the system asks you to register with the syst em operator by entering your n ame and locat ion. The s ys tem operator will set up your acc ess acco unt within 24 hour s. A t th at time, y ou can access the fil es on the BB S. NOTE If you enco unter any difficulty ac cessin g the highspe ed m odem, try the dedicated 240 0baud modem. T o acc ess the fil es, complet e these steps 1. Enter F from the B BS Main menu. The B BS displ ays the list of area s and prompts for t he a rea number. 3. T ype 12 and press to selec t MCS 96 Fami ly.T o acce ss the fil es, complete t hese steps 1. T ype F from the BB S M a in menu. The BB S displa ys t he ap prox imate t i me required to download t he selected f i les and gi ves you th e option to d ownload them. 1.4.3 Comp uServe Foru ms The Comp uServe forums pro vide a means for y ou to gather information, share discoverie s, and debate issues. T y p e “go i nte l” for ac cess.C la sses are held in the U.S. 1 80023 48806 U.S. a n d Canada NOTE This manua l de scribes a family of device s. For brevi ty, the name 8XC196K x is used whe n the disc ussion a pplies t o all fami ly membe rs. W hen informa tio n applies to specific devices, individual product names ar e used. 2.1 T YP ICAL APP LICA TIO NS MCS 9 6 microcont r ollers are t ypic ally use d fo r highspee d eve nt cont rol sys tems.

Comme rcial applica tions inc lude modem s, moto r control syste ms, printers, photocopie rs, air condi tioner con trol syste ms, disk drives, and m edical instrume nts. Aut omotive c ustome rs use MC S 96 microcon trolle rs in e nginec ontr ol syste ms, a irba gs, suspensi o n system s, and antiloc k braki n g system s ABS. The core of the device Figure 22 consist s of the centra l processing unit CPU and me mory controll e r. The CPU contains the regis ter file and the regi st er arithm eticlogi c uni t RAL U . The CPU c onne cts to bot h the me mory cont roller and an interrupt c ontroll er via a 16bit inte rnal b us. An exte nsion of this b us connects the C PU to the inte rnal periphera l modules. In addit ion, a n 8bit internal bus transfers instructio n bytes from the memory co ntroller to the inst ruct ion register in the RALU. Th e 87C1 96 CA, 8XC1 96 JQ, JR, KQ, KR, a nd KT are o ffere d in both autom otive a nd comm ercia l tempera tu re ran ges. 4. T he 87 C1 96CA a lso h as a n onchip n etworkin g perip heral that sup ports CAN sp ecifi cati on 2.0. Port Interrupt Controller CAN Note. The slave port is unique to 8XC196K x devices. The CAN peripheral is unique to the 8XC196CA. A279701 Register File Register. RAM CPU SFRs RALU Microcode. Engine ALU Master PC Memory Controller Prefetch Queue Slave PC Address Register Data Register CPU Bus Controller PSW Registers The mic roc ode e ngine dec odes the instruct ions a nd t hen gene rat es the seq uence of events tha t cause desi red functi ons t o occur. 2.3.2 Regi ster File The regis te r file is divi ded i nto an upper a nd a lowe r fil e. I n the lower re gist er fi le, the l owest 24 bytes are alloca te d to the CPU ’ s spe cial f u nc tion regist ers SFR s and the s tack point er, whi le the remai nder is available as generalpurpose register R AM. T he up per register file contai ns only generalpurpose register RAM. The re gister R AM ca n be accesse d as bytes, words, or double wor ds.

The RAL U ac cesses the upper and lower regis ter file s dif fe rentl y. The lowe r regist er fi le is alway s direct ly access ible with registerdirect addressi ng see “Addressi ng Modes” on page 35. The upper register fi le is accessible with registerdirect a d dressing only when windowi ng is e nab led. W in dowin g is a technique that ma ps blocks of the up per register file into a window in the lowe r register file. See Chapter 4, “ Me mory Partitions, ” for more in formation ab o ut the register file and windowing. 2.3.3 Register Ari thm eticlo gi c Unit RALU The RAL U cont ains the microcode

engine, the 16bit arithme tic logic unit A LU, the m aster p ro gram counte r PC, the progr am sta tus wo r d P SW, and se veral regi st ers. The regi sters in the RALU are t he instr uction regist er, a c o nstants regi ster, a bitselec t regist er, a loop counter, a nd three temp orary registers the upperword, lowerword, and se co ndoperand r egis ters. The PSW co ntains one bit PSW. 1 that globall y enabl es or disa bles servi cin g o f all ma skabl e in terr upts, one bit PSW.2 that ena ble s or disable s the perip heral transac tion serve r P TS , and si x Boolea n flags that reflec t the s tate of your program. Appendix A, “Instruction Set Reference” provi des a detailed desc ript ion of t he PSW. All re gisters, e xcept the 3bit bi tse lect re gister and the 6bit l o op counte r, a re either 1 6 or 17 bits 16 bits plus a sign extensi on. Som e of t hese r egis ters can reduce the A LU’ s workload by per form ing s imple o perations. These regi sters ha ve thei r own shift logic and are use d for operatio ns that require logical shifts, incl uding norm alize, multiply, and divide operati ons. The sixbit loop coun t er counts repetitive shi fts. The secon d operan d register stores the se cond operand for twoopera nd instruct ions, i ncl uding the mul tiplier d urin g mult iply operat ions and the divis or during divide operations.

During sub t raction operatio ns, t he output of th i s register is co m plement ed befo re i t i s move d into t he A L U. The RA LU spee ds up calcula tions by storing constant s e.g., 0, 1, and 2 in the co nstants regi ster so that they are rea dil y availabl e when complem enti ng, increme nti n g, o r decre me nting bytes or wo r ds. I n a ddition, the co nstants regi st er genera tes singlebit mas ks, base d on the bitsele ct reg ister, for bittest inst ructio ns. 2.3.3.1 Code E xecution The RAL U per f orms most c alcul ations fo r the device, but it does not us e an acc um ul at or. Inst ead it operat es direc t ly on the lowe r regist er fi le, w hich e sse nti ally prov ides 2 56 accu m ul a tors. Be cause da ta does not flow through a single accumul ato r, the devic e’ s code exec ute s faster and m ore efficient ly. 2.3.3.2 Instruction F ormat MCS 96 m icroco ntrollers combine a la rg e set of generalpurpose regis ters wi th a three operand instruct ion f ormat. This forma t allows a single instr uction to spe cify two s ource regist ers an d a separat e desti nation regist e r. For example, the followi ng instructio n m ultiplie s two 16bit vari ables and stores the 32b i t result i n a third vari able. The f ollowi ng ex ample shows the equiva lent code f o r an 80C186 device.The b us controlle r rec eives m emoryac cess re q uests fr om either the RALU or the prefetch queue; q ueue requests always ha ve priority. Thi s queue is transparent to the RALU and your soft ware. NOTE When using a l ogic a nal yzer to deb u g code, remem ber that i nstruc tio ns are preloaded int o the prefetc h queue and a re not nece ssari ly execute d imme dia tely after they are fetched. When the bus controller re ceives a req uest from the queue, it fetches t he code from t he addres s containe d in the slave PC.

The slave PC increa se s exec uti on spe ed bec ause t he next inst ruct ion byte is availabl e immediate ly an d the processor need not w ait for the master PC to send t he ad dress to the m em ory controll er. If a jump, int errupt, call, or ret urn chan ges the address seque nce, the mast er PC l oads the new address into the slave PC, then the CPU flushes the queue an d con tinues processing. 2.3.5 Interru pt Ser vic e The de vice’ s flexible interrupthandl ing syst em has two main com ponents the programma ble in terr u pt control ler and t he peripheral transac tion s erver P T S. The p rogrammable inte rrup t con troller has a hardware priority scheme that c an be modified b y your software. Interrupts that go throug h the int errupt control ler are serviced by i nterrupt servi ce routines that you prov ide. Th e peripheral t ransact ion server P TS, a microco ded hardware interrupt processor, p rovides high speed, lowoverhea d interrupt handling. Y ou can configure most interrupts except N M I, trap, and unimple me nte d o p code t o be se rviced by t he P TS inst ead of t he int errupt controll er. Se e Chapt er 5, “ Stan dard and P TS Inte rr upts,” for more in forma tion. T he clock ge nerato rs a ccept the divi ded input frequency from t he di videbytwo circuit an d produ c e two n onoverlapping interna l timing signals, P H 1 and P H 2. These signal s are ac tive when hi gh. T he ri sing edges of PH1 and PH2 gen erate CL KO UT, the output of the i nte rnal clock gene rator Fi gure 24 . The cloc k circuit ry routes separat e inte rnal clock s ignals to the CPU and t he

peripheral s to prov ide flex ibili ty in po w er man agement. “Reduc ing Power Co nsumptio n” on page 143 describes the power ma nagem ent modes. It also outputs the CLKOUT s ignal on the CLKOUT pin. B eca use of the comple x logic in the c lock circui try, the signa l on the C LKO UT pin is a delayed version of the interna l CLKOUT signal.

This de lay vari es with t empera ture and vol tage. Figure 2 3. Clock Circuit ry A306402 Clock. Generators CPU Clocks PH1, PH2 Dividebytwo. Circuit Peripheral Clocks PH1, PH2 CLKOUT Disable Clocks Powerdown Disable Clocks Idle, Powerdown XTAL1 XTAL2 F OSC Disable. Oscillator Powerdown Disable Clock Input Powerdown T abl e 2 2 l ist s s tate time durations at va rious frequencies. The followi ng formula s c alcul ate the frequency of PH1 a nd PH2 and the duration of a state t ime F OSC is t he input fre quency to the divide bytwo circui t. Because the de vic e can opera te at ma ny freque nci es, this ma n ual define s time require me nts in terms of st ate t imes rather than spec ifi c t imes. C onsult the lat est da tashee t for AC timi ng specifi c ation s. 2.5 INTERNAL P ERIPHERAL S The inte rnal periphe ral modules provide spec i al functio ns for a variety of appl ications. Thi s sec tion provides a brief des cript ion of each peri p heral and othe r chapt ers descri be e ach one in det ail.Port 5 provides bus c ontrol sig nals; for the 8 X C196K x, it c an al so provide pins for the slave port. NOTE The 87C196C A device does not imple me nt t he f o ll owing port p ins P0.10, P1.74, P2.5 and P2.3, P5.7 an d P5.1, and P6.32. See “Des ign Conside rations for 87C196CA De vices” on page 2 13 for det ails. The UAR T has one synchr onous mode mode 0 and three asynchronous modes mo des 1, 2, and 3 for both transmission and rece ption. The asynchronous modes are full du plex, meaning tha t they can trans mit and rec eive dat a simult aneousl y. The re ceive r is buffered, s o the recept ion of a seco nd byte may begi n before the first byte is read. The transmi tter is also buff e red, a llowing c ontinuous tra nsmissi ons. The channel s can be programmed to operate in s evera l modes.How ever, it is relatively slow a nd involves software o verhead to diff erent iate data, addresses, and commands.